AMENDMENTS TO THE SPECIFICATION:

At page 1, starting on line 3, please change the subtitle to read as follows:

A3

1. ~~Filed~~ Field of the Invention

At page 17, paragraph 3, starting on line 10, please change to read as follows:

A4

Figure 1 is a ~~schmematic~~ schematic view of a first embodiment of an information processing device according to the present invention which performs pipeline processing, and Figure 2 shows a basic form of an instruction sequence comprising a branching instruction. This basic form of an instruction sequence is a configuration of instruction sequence C1 extending from instruction 01 to instruction 08, instruction sequence C2 extending from instruction 11 to instruction 16, instruction sequence C3 extending from 41 to 46, and instruction sequence C4 extending from 21 to 28. In addition, the instruction sequence in Figure 2 comprises branching instruction 02 which branches to instruction sequence C2, branching instruction 04 which branches to instruction sequence C3 and branching instruction 12 which branches to instruction sequence C4.

At page 21, paragraph 2, starting on line 8, please change to read as follows:

A5

The instruction buffering portion 12 supplies to the decoder 21, from one of the instruction buffers e-1 or e-2, the instruction which, on the basis of the branching prediction of the branching prediction portion 13, is predicted to be the next to be executed. In this case, the branching prediction of the branching prediction portion 13 is, for example, performed with reference to the hint bit which indicates the branching priority level associated with the branching instruction. In addition, when it has become apparent that the instruction sequence (for example C1 or ~~C~~ C2) which is buffered in the instruction buffering portion 12 e-1 or e-2 is not

A5 being used as a result of the branching of a branching instruction or the like being determined, the instruction sequence which is buffered at that time is invalidated, so that the branch target instruction sequence which is newly read (for example C4 or C3) can be buffered. Furthermore, a bypass route 24 which supplies the instructions read from the instruction store 11 to the decoder 21 without passing through the instruction buffers e-1 and e-2 is provided in the instruction buffering portion 12. By this means it is possible to supply the read instruction immediately to the execution unit 20.

At page 28, last paragraph, starting on line 21, please change to read as follows:

A6 Figure 5 shows the timing chart of the case in which the branching route (1) shown in Figure 4 has been executed by the information processing device according to an embodiment of the present invention. The signals P, T, C, D, E, W of each of the cycles in Figure 5 represent the ~~5~~ 6 stages of the pipeline processing for one instruction, and an explanation of the contents of the processing of each stage will be given first.

At page 30, paragraph 2, starting on line 9, please change to read as follows:

A7 Of the ~~5~~ 6 aforementioned stages, it is the consecutive execution operations of the execution stage E which make it possible to perform pipeline processing without pipeline processing confusion and to make most efficient use of the resources of the instruction execution unit 20.

At page 33, last paragraph, starting on line 21, please change to read as follows:

A8 In this case, the instruction sequence which follows branch target instruction 11 is

buffered in the empty instruction buffer e-2. However, even though the instruction buffer e-2 is empty, if the branching possibility level of branching instruction 02 is low, it is not necessary to store the branch target instruction sequence 11-16 of branching instruction 02 in instruction buffer e-2 simply because the branch target address information of branching instruction 02 is stored in the first branch target address information register b-1.

At page 49, paragraph 2, starting on line 9, please change to read as follows:

The cache memory unit 50 comprises the cache memory unit 52 and the cache controllers 54, 56. The cache controllers 54, 56 ~~fetches~~ fetch instructions from the cache memory 52 or the main memory 64 depending on the fetch request S20 from the instruction fetch portions 410, 411. Accordingly, the cache memory unit 50 becomes a 2 port unit which can receive both sequential side and target side instruction fetch requests at the same time. The cache controllers ~~controller~~ 54, 56 ~~allocates~~ allocate addresses AD to the cache memory and ~~fetches~~ fetch instructions. Then, the hit/miss CHM signal which indicates whether there has been a cache hit or a cache miss with those instruction fetches is transmitted back to the respective controllers 54, 56 from the cache memory 52.